What is claimed is:

1. A method of manufacturing a flash memory device, comprising the steps of:

(a) providing a semiconductor substrate in which a gate electrode including a tunnel oxide film, a floating gate, a dielectric film and a control gate is formed; and

(b) implementing a dry oxidization process using a mixed gas of O_2 and $C_2H_2Cl_3$ to form sidewall oxide films at the sidewalls of a gate electrode in order to compensate for damage due to an etch process for forming the gate electrode and reinforce isolation of the floating gate.

2. The method as claimed in claim 1, wherein the step (b) comprises:

loading the semiconductor substrate onto a deposition chamber;

raising the temperature inside the deposition chamber to a first temperature;

introducing an O_2 gas of 1 ~ 10slm and a $C_2H_2Cl_3$ gas of 0.1 ~ 1slm into the deposition chamber at the first temperature to form a sidewall oxide film; and

unloading the semiconductor substrate from the deposition chamber.

3. The method as claimed in claim 2, wherein the first temperature is 750 ~ 950℃.

4. The method as claimed in claim 1, wherein the sidewall oxide films are formed in thickness of 30 ~ 100 Å.

5. The method as claimed in claim 1, wherein the step (a) comprises:

sequentially forming a tunnel oxide film, a first polysilicon film and a pad nitride film on the semiconductor substrate;

etching the pad nitride film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate through a patterning process to form a trench within the semiconductor substrate;

depositing an oxide film on the entire structure including the trench and then polishing the oxide film so that the pad nitride film is exposed;

etching the pad nitride film and then depositing a second polysilicon film on the entire structure;

patterning the second polysilicon film to form a floating gate;

depositing a dielectric film on the entire structure along its step; and

forming a material film for a control gate on the dielectric film and then implementing a patterning process to form the control gate.